



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/500,607	02/04/2000	Robert David Koudelka	MSC-22875-1	2853

24957 7590 01/29/2003

NASA JOHNSON SPACE CENTER  
MAIL CODE HA  
2101 NASA RD 1  
HOUSTON, TX 77058

EXAMINER

BOCURE, TESFALDET

ART UNIT	PAPER NUMBER
----------	--------------

2631

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/500,607	<b>Applicant(s)</b> KOUDELKA, ROBERT DAVID	
	<b>Examiner</b> Tessfaldet Bocure	<b>Art Unit</b> 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 February 2000.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 23 is/are allowed.
- 6) ☐ Claim(s) 1-3,6-13,15-20 and 22 is/are rejected.
- 7) ☐ Claim(s) 4,5,14 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2</u> . | 6) <input type="checkbox"/> Other: _____                                    |

Art Unit: 2631

## DETAILED ACTION

### *Information Disclosure Statement*

The Examiner has considered the information Disclosure Statement received on 02/04/00 and the initialed copy (one copy) of the 1449 is attached with this correspondence.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3,6-12,13,16-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by **Bath et al.** (US patent number 5,909,149).

**Bath et al.** (**Bath** hereinafter) teaches a multiband phase locking loop comprising : a frequency range detector (not shown in figures 1 and 4) for generating a selected band (see band selected input to the PLL in figures 1 and 4) having a frequency range of 894-964 and 120-2060 (claimed range in claims 3,6,7,11,12, 18 and 19) for controlling the PLL (19) circuit to phase lock the received signal (fref) having the selected frequency ranges with that of the internally generated clock signal (claimed synchronizing the input signal in claims 13 and 20) as in claims 1,9 and 16.

Further claims 2,10 and 17, **Bath** also teaches that the output signal from the oscillator 12 and 14, which is phase corrected (claimed conditioning claims 8,15 and 22) by the divider (20).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2631

4. Claims 1,2,6-12,13,16-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by **Borwn et al.** (US patent number 5,119,043).

**Borwn et al.** (**Borwn** hereinafter) teaches a multiband phase locking loop (fig. 1) comprising : a frequency range detector (30 and 32) for generating a selected band (see input N ) having a frequency scaling value (claimed range in claims 3,6,7,11,12,18 and 19) for controlling the PLL (19) circuit to phase lock the received signal having the selected frequency ranges with that of the internally generated clock signal (claimed synchronizing the input signal in claims 13 and 20) as in claims 1,9 and 16.

Further claims 2,10 and 17, **Borwn** also teaches that the output signal from the oscillator 20 (claimed conditioning input wave having oscillator in claims 8,15 and 22) is divided by the divider (34).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1,2,6-12,13,16-20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by **Harrer** (US patent number 6,091,304).

**Harrer** teaches a multiband phase locking loop (figs .1 and 7) comprising : a frequency range detector (180,116) for generating a selected band (see input 116 and 117 ) having a frequency range (claimed range in claims 3,6,7,11,12,18 and 19) for controlling the PLL (19) circuit to phase lock the

Art Unit: 2631

received signal having the selected frequency ranges with that of the internally generated clock signal (claimed synchronizing the input signal in claims 13 and 20) as in claims 1,9 and 16.

Further claims 2,10 and 17, **Harrer** also teaches that the output signal from the oscillator 140 (claimed conditioning input wave having oscillator in claims 8,15 and 22) is divided by the divider 150.

### ***Allowable Subject Matter***

7. Claim 23 is allowed.

8. Claims 4,5,14 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The claimed subject matter in claims 4,5,14 and 21 is allowable because the arts of record fail to teach or fairly suggest the claimed "a wideband phase lock loop comprising: a frequency detector to detect the frequency information of an input signal, the frequency detector having a zero-crossing synchronizer (22a) (as in claims 23 and 4) for synchronizing the input signal to a clock signal and a zero-crossing counter (22b) for counting zero-crossing of the input signal (as in claims 5,14 and 21); and in combination with the frequency range selector responsive to the zero-crossing counter and synchronizer for selecting the frequency range of the input signal, phase lock loop, divider and voltage comparator as in claim 23."

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US patent numbers 4,229,827; 4,302,845; 4,660,182; 5,963,068 and 6,215,834 issued to Bowman, McClaughry et al., Bates et al., Hardesty et Al., and McCollough respectively disclose a multi-band PLL circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tesfaldet Bocure whose telephone number is (703) 305-4735. The examiner can normally be reached on Mon-Thur (7:30a-5:00p) & Mon.-Fri (7:30a-5:00p).

Art Unit: 2631

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 305-3988 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

T.Bocure  
January 26, 2003.

Tesfaldet Bocure  
Primary Examiner  
Art Unit 2631

